REMARKS

Claims 1-44 are pending in the present application. Claims 6, 19, 32, and 35 have been amended to correct errors missed in the previous amendment.

The specification is objected to under 35 U.S.C. §112, 1st paragraph. Applicant respectfully disagrees for the reasons given below.

Claims 1-44 are rejected under 35 U.S.C. §112, 1st paragraph, as failing to comply with the enablement requirement. Applicant respectfully traverses this rejection for the reasons given below.

Claims 1-44 stood rejected under 35 U.S.C. §103(a) as being unpatentable over Rowlands (U.S. Patent Application Publication No. 2003/0217216) (hereinafter "Rowlands"). Applicant respectfully traverses this rejection for the reasons given below.

Objection to the Specification under 35 U.S.C. §112, 1st paragraph

In paragraph 5 of the present Office action, the Examiner asserts the specification is replete with terms that are not clear, concise, and exact and thus is objected to under 35 U.S.C. 112, 1st paragraph. Applicant respectfully disagrees. More particularly, the Examiner asserts in the sole example, that nowhere in the specification are the specifics of terms such as proxy read to own (PRTO) packets and proxy invalidate (PI) packets described. The Applicant respectfully disagrees with the Examiner. More particularly, the description, at paragraphs [00249] through [00255], describes the embodiment using the PRTS and PRTSM packets as recited in claims 3-5. In addition, in paragraph [00249] the specification discloses

> "A transaction initiated within a node may cause certain ownership and/or access right changes within that node during the transaction, but the gTag of the requested coherency unit may not be updated until later in the transaction."

The specification also discloses at paragraph [00203] and similarly in [00211]

> "Similarly to an RTO transaction in a single-node system, receipt of the PRTOM response causes owning device D2 to lose ownership of the coherency unit. D2 also sends a copy of the coherency unit to interface 148H in response to receiving the PRTOM packet."

The specification also discloses at parapgraph [00221]

> "A device D1 initiates a RTO transaction for a coherency unit whose home node is home node 140H. In this embodiment, packets for the requested coherency unit are conveyed in PTP mode in home node 140H. Thus, the RTO request packet is conveyed to memory subsystem M. Memory subsystem M (or, in one embodiment, the address network in home node 140H) returns an RTO response to the requesting device D1, causing the requesting device to gain an ownership responsibility for the requested coherency unit. However, since the home node is gS for the requested coherency unit, the memory subsystem cannot complete the RTO transaction by providing D1 with data."

The specification also discloses at paragraph [00238]

> "In some embodiments, a multi-node system 100 may be configured so that if a static coherency unit is gM in one node, no other node in the multi-node system is a gS or gM node for that coherency unit. Conversely, if any node is gS for the coherency unit, no node is gM for the coherency unit."

The specification also discloses in paragraph [0250]

> "In order to cause memory to respond to the RTS while not removing ownership from the device D2 that initiated the subsequent RTO, the interface may use a special type of proxy read-to-share (PRTS) address packet. In one embodiment, there may be two types of proxy request packets. One type may be used in non-gM nodes and the other may be used in gM nodes. In this description, gM-type packets are identified by an "M" at the end of the packet identifier (e.g., PRTOM, PRTSM, and PIM) and non-gM-type packets lack the "M" identifier (e.g., PRTO, PRTS, and PI). The non-gM type of request packets may cause memory to respond, even if it is not the current owner, and not affect the ownership of owning caches within a node. In contrast, the gM type of packets cause owning active device to give up ownership and are not responded to by non-owning memory subsystems." (Emphasis added)

From the foregoing disclosures, Applicant submits it is possible for two or more active devices within two or more different nodes to instantaneously have ownership

responsibility within their respective nodes. However, as disclosed above, the system will not allow more than one device to have access to the data without invalidating all other copies. Thus, the embodiments described above do allow for a device to request (via, for example, an RTO) and obtain ownership. For example, using the above disclosure it is possible for a coherency unit to gS in all nodes, including a home node. If an active device sends an RTO on the local address network, all other copies must be invalidated, but the interface or the memory subsystem will send an RTO response to the device, giving it ownership responsibility before the actual data is delivered. Now, if another device in a remote node also does an RTO and prior to the home node request, that device's interface or memory may also do an RTO response giving that device ownership responsibility, and then queue the request in an outstanding request queue. When the home node receives the coherency message from the remote node, since the coherency unit is still gS in the home node, the home node interface will send a PRTO on the address network. To which the device in the home node having the ownership will ignore and the memory subsystem will respond with data, while not causing the active device in the home node to lose ownership. The coherency unit will change state to gM in the remote node once all shared copies are invalidated and the requesting remote device receives the data and provides an acknowledgement to the home node.

Thus, the owning device ignores the non-gM-type of packet, and lets the memory subsystem respond. Examples of these types of packets are given above in paragraph [00250] and include (e.g., PRTO, PRTS, and PI). The gM-type packets include (e.g., PRTOM, PRTSM, and PIM). Accordingly, paragraph [00250] in combination with the description of the embodiment described in paragraphs [00252]-[00255] as well as the other paragraphs both shown above and in the specification support the claim language. Accordingly, Applicant respectfully requests the Examiner withdraw the objection to the specification based on 35 U.S.C. §112, 1st paragraph.

Rejection of the claims under 35 U.S.C. §112, 1st paragraph

The Examiner asserts the claim language contradicts itself because the specification (per paragraph 90) defines an "owner" of a coherency unit to be responsible

for providing data to another client which requests that coherency unit, and the claim language (e.g., claim 1) recites ignoring the address packet. The Examiner asserts the claim language and the specification contradict one another.

Applicant respectfully disagrees and maintains arguments previously presented in the response filed July 9, 2007. Specifically, Applicant submits the definition of the "owner" given in the written description does not preclude other operation, as is clearly evidenced in portions of the specification. However, in an effort to explain, Applicant directs the Examiner's attention to paragraphs [00249-00255] of the specification and Fig. 32, in which an embodiment is describe regarding PRTS and PRTSM packets. The embodiment described therein clearly illustrates a case in which an active device (D2) in the home node obtains ownership responsibility (via issuing an RTO packet which has not yet been serviced), ignores a PRTS packet, and the memory subsystem in the home node responds to the PRTS packet by sending the data, because the coherency unit is still considered non-gM (i.e., gS) in the home node at that time. The specification further describes the case where if the RTO packet were serviced prior to the PRTS being serviced in the home node, then the PRTS packet would become a PRTSM packet, in which case the owning device (i.e. D2) would respond and provide the requested data. Thus, claim 1 is clearly enabled by the specification.

Furthermore, in regard to the Examiner's rejection of claims 7-12, 20-25, and 36-41, as described above, at least paragraph [00250] of the specification provides adequate support. Accordingly, Applicant respectfully requests the Examiner withdraw the rejection based on 35 U.S.C. §112, 1st paragraph.

Rejection under 35 U.S.C. §103(a)

The Examiner asserts "In view of the ambiguities stated above Rowlands *appears* to teach limitations of claims 1-44." The Examiner further asserts "With respect to remaining limitations of claims, such as sending first type of address packets and second type of address packets depending upon the global states the applicant's disclosure is failed to properly describe such packets as explained above with respect to rejection of

claims under indefiniteness and Rowlands teaches a multi-node system with dual level of coherency..."

Applicant respectfully points out the claims are not currently rejected for indefiniteness, and further points out the claims are definite, since there are circumstances in which an owner can and does have ownership if the coherency unit is not yet in the gM state (see above discussion). It's all in the timing of the requests and their processing.

Further the Examiner asserts Rowlands teaches the remaining limitations (first and second types of packets) at paragraph [0035]. However, Rowlands actually discloses at paragraph [0035]

> "[0035] ... As used herein, the "state" of a cache block in a given node refers to an indication of the ownership that the given node has for the cache block according to the coherency protocol implemented by the nodes. Certain levels of ownership may permit no access, read-only access, or read-write access to the cache block. For example, in one embodiment, the modified, shared, and invalid states are supported in the internode coherency protocol. In the modified state, the node may read and write the cache block and the node is responsible for returning the block to the home node if evicted from the node. In the shared state, the node may read the cache block but not write the cache block without transmitting a coherency command to the home node to obtain modified state for the cache block. In the invalid state, the node may not read or write the cache block (i.e. the node does not have a valid copy of the cache block). Other embodiments may use other coherency protocols (e.g. the MESI protocol, which includes the modified, shared, and invalid states and an exclusive state in which the cache block has not yet been updated but the node is permitted to read and write the cache block, or the MOESI protocol which includes the modified, exclusive, shared, and invalid states and an owned state which indicates that there may be shared copies of the block but the copy in main memory is stale). In one embodiment, agents within the node may implement the MESI protocol for intranode coherency. Thus, the node may be viewed as having a state in the internode coherency and individual agents may have a state in the intranode coherency (consistent with the internode coherency state for the node containing the agent)."

From the foregoing, Rowlands is merely disclosing that a cache block may have different coherency states based on the internode coherency protocol or the intranode

coherency protocol. However, it does not teach sending a different type of packet. Thus, Applicant submits, Rowlands does not teach or suggest "... in response to receiving from the additional node via the inter-node network, a coherency message requesting an access right to a coherency unit, the interface is configured to send a first type of address packet on the address network if a global access state of the coherency unit in the node is a modified state and to send a second type of address packet on the address network if the global access state of the coherency unit in the node is not the modified state," as recited in claim 1. More particularly,

In addition, the Examiner asserts Rowlands teaches "if the given active device has an ownership responsibility for the coherency unit, the given active device is configured to ignore the second type of address packet and to respond to the first type of address packet," as recited in claim 1 at paragraph [0058] because "a single transaction (command) may be used for probes or there may be a probe generated transaction that invalidates agent copies of the cache block and another probe-generated transaction that permits agents to retain shared copies of the cache block." Applicant is unsure of what the Examiner is alluding to with that statement. However, Applicant submits Rowlands actually discloses at paragraph [0058]

> "[0058] The RdKill and RdInv transactions may be used by the memory bridge 32 in response to probes received by the node 10 from other nodes. The RdKill and RdInv transactions cause the **initiator (the memory bridge 32)** to acquire exclusive access to the cache block and cause any cache agents to invalidate their copies (transferring data to the initiator similar to the RdShd and RdExc transactions). In one embodiment, the RdKill transaction also cancels a reservation established by the load-linked instruction in the MIPS instruction set, while the RdInv transaction does not. In other embodiments, a single transaction may be used for probes. In still other embodiments, there may be a probe-generated transaction that invalidates agent copies of the cache block (similar to the RdKill and RdInv transactions) and another probe-generated transaction that permits agents to retain shared copies of the cache block." (Emphasis added)

Applicant is unclear from the foregoing disclosure, how Rowlands teaches the above limitation. In addition, Rowlands is teaching the memory bridge 32 performing the above actions, and the Examiner asserts in the rejection that the interface 20 in

Rowlands corresponds to Applicant's claimed interface. Further, Applicant submits although Rowlands teaches various coherency protocols and ways of handling local and remote transactions, Rowlands does not teach or suggest "in response to receiving from the additional node via the inter-node network, a coherency message requesting an access right to a coherency unit, the interface is configured to send a first type of address packet on the address network if a global access state of the coherency unit in the node is a modified state and to send a second type of address packet on the address network if the global access state of the coherency unit in the node is not the modified state" or "if the given active device has an ownership responsibility for the coherency unit, the given active device is configured to ignore the second type of address packet and to respond to the first type of address packet," as recited in Applicant's claim 1.

Lastly, Applicant questions the propriety of a rejection under 35 U.S.C. §103(a). The Examiner has in no way provide a *prima facie* case of obviousness. The Examiner has merely stated that the limitations *appear* to be taught by the references. (Emphasis added)

Thus, Applicant submits claim 1 along with its dependent claims, patentably distinguishes over Rowlands for the reasons given above.

Applicant's claims 15, 31, and 44 include features that are similar to the features recited in claim 1. Thus, Applicant submits claims 15, 31, and 44 along with their respective dependent claims, patentably distinguish over Rowlands for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5181-95101/SJC.

Respectfully submitted,

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